7SG12 DAD N

Numerical High Impedance Relay with CT Supervision

Document Release History

This document is issue 2010/02. The list of revisions up to and including this issue is:
Pre release

2010/02.	Document reformat due to rebrand

Software Revision History

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1. Introduction

These notes give guidance on the application of the DAD-N. Reference should also be made to the Commissioning section, which provides detailed set-up instructions.

2. Differential Protection

A Busbar is a zero impedance connection joining several items such as lines, loads etc. Therefore at busbar stations the switchgear is stressed, at times of fault, to levels higher than occur elsewhere on the system. It is therefore important that faults are detected and cleared as quickly as possible. In addition, since Busbars act as connection points in an electrical system, it is important that good fault discrimination is achieved with only the minimum amount of plant necessary to clear the fault being disconnected.

Differential unit protection is the most obvious solution to these requirements.

Differential protection works on the basic premise that the currents which enter a protection zone should be equal to the currents leaving it. Any discrepancy, allowing for measuring errors, etc. indicates an in-zone fault. By contrast an external fault will produce no discrepancy in the measured currents.

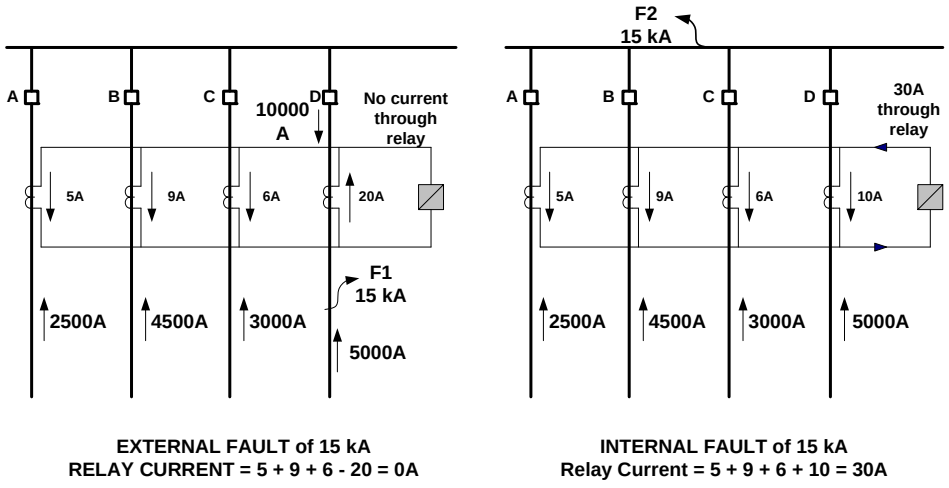


Figure 1 – Current Differential Protection

Good fault discrimination is achieved, therefore. In addition, because the protection is based on simple current level detection it is extremely fast. Typical operate time for a high impedance scheme is <20ms.

Busbar faults are almost always permanent faults and are therefore not suitable for Auto-reclosure. Instead every source connection to the Busbar must be broken and isolated.

3. High Impedance Differential Protection

In a High Impedance current differential scheme, the secondary winding of the CTs positioned at all entry and exit points of a protected zone are summated external to the protection relay. These entry and exit points must include all incomers, sections, couplers and outgoing feeders. The principle is therefore that one protection Relay must be provided for each protected zone.

The principles of such a scheme can easily be extended to a 3-phase system. In effect three separate protection circuits, each covering one phase, are installed. Each phase system is joined together at the star point of each set of CTs with the star point always connected away from the protected zone. These will provide both phase-phase and phase-earth coverage.

The High Impedance Busbar protection must satisfy 2 criteria:

- It must be **stable** so that operation does not occur for any faults external to the protected zone.
- It must be sufficiently **sensitive** so that any faults in the protected zone are detected.

To achieve **stability**, the protection must be designed so that it is tolerant to any current imbalances due to CT saturation effects resulting from external (through) faults. Transient stability under through fault conditions is a problem with many forms of differential protection due to variations in CT magnetising characteristics. As saturation is approached, the CT output current waveforms become increasingly distorted with a high percentage of 3rd and other higher odd harmonics. These variations can lead to unbalanced currents causing mal-operations.

3.1 Stabilising Resistor

Consider a simple 4 CT protection:

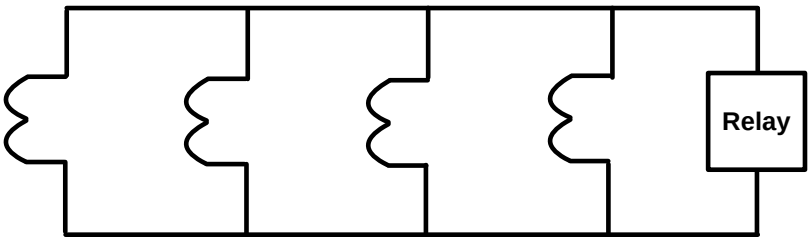


Figure 2 – Simple 4 CT Protection

It is a proven design principle that the worst case for current unbalance due to CT saturation occurs when one of the paralleled CTs becomes completely saturated while all the other CTs continue to function linearly. This situation would never occur in reality, but by making the protection tolerant to it we can be confident that it will remain stable for all through fault conditions.

When a CT becomes total saturated, its secondary winding can be considered as a resistance rather than a current source. The value of this resistance is equal to the CT secondary resistance, R_{ct}, and will be considerably larger than the resistance of the Relay analogue inputs. This means that most of the unbalanced currents from the other CTs will flow through the Relay and these may be of sufficient magnitude to operate the protection.

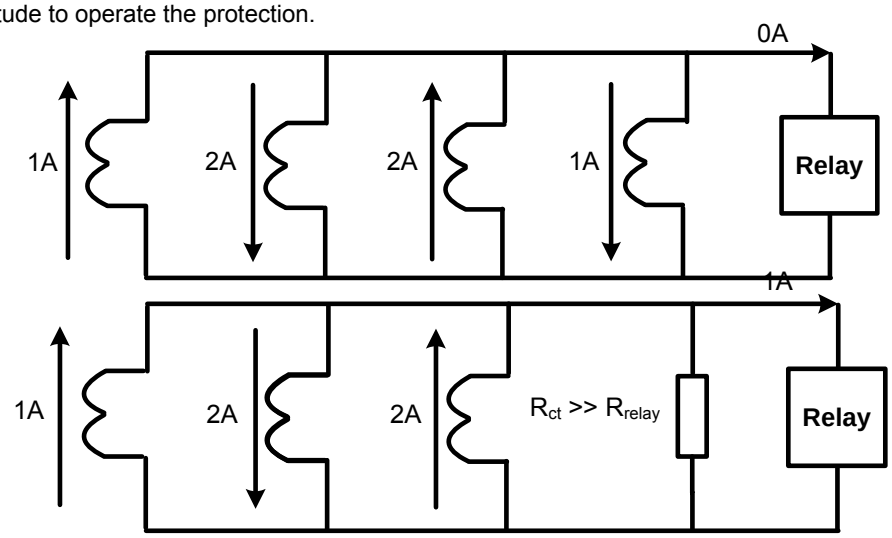


Figure 3 – Current Distribution with one CT totally saturated

The solution is to load the Relay circuit by adding a series resistor such that most of the unbalance current due to the CT becoming saturated will instead flow through the saturated CT secondary. Since this resistor will make the protection stable for all through faults, it is termed the Stabilising Resistor, Rstab. Similarly, it is this additional resistance which makes the Relay a “High Impedance” path.

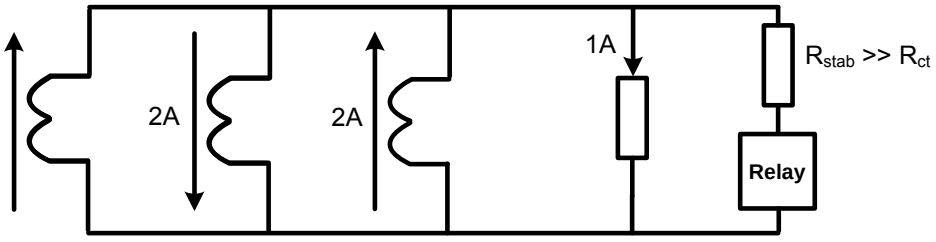


Figure 4 – Stabilising Resistor

The maximum voltage which can appear across the Relay for a through fault coincident with CT saturation is:

$$V_{max}\,(V) = I_{MaxSecExtFault}\ x\ (R_{ct} + (2\ x\ R_{lead}))$$

Where:

$I_{MaxSecExtFault}$ = Maximum secondary external (through) fault current = $I_{MaxPriExtFaul}$ x CT Ratio

R_{ct} = CT secondary winding resistance

R_{lead} = Maximum lead resistance in parallel with the Relay circuit

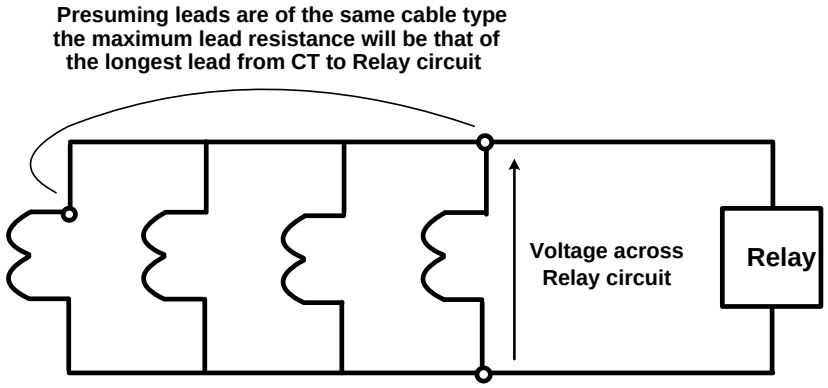


Figure 5 – Measuring Lead Resistance

So that R_{lead} + R_{ct} + R_{lead} is the total resistance in parallel with the Relay.

There will be some lead resistance between the Relay and the closest CT, but this is generally ignored to give the most onerous operating conditions.

If $I_{MaxPriExtFault}$ is not known, the breaking capacity current of the Circuit Breaker can be used.

The value of R_{stab} must be such that the current flowing through the Relay at this voltage is less than the protection pick-up setting, I_s.

I_s must be chosen so that the protection will operate for all internal fault currents. **Sensitivity** is achieved by ensuring that I_s is such that the protection will operate at the correct level of primary fault current. See Section 3.3 “Fault Setting”.

Therefore, for stability:

$$\frac{V_k}{2} x \frac{1}{I_s} \geq R_{stab}\,(\Omega) \geq \frac{V_{max} - V_{relay}}{I_s}$$

Where:

V_{relay} = The burden of the Relay analogue inputs (VA) / nominal current (A)

For the DAD-N, this will be so small that it can be ignored

Usually the value of R_{stab} is chosen at the higher end of the range, so that:

$$\frac{V_k}{2} x \frac{1}{I_s} \geq R_{stab}\,(\Omega) \geq \frac{V_k}{4} x \frac{1}{I_s}$$

The Voltage across the Relay and Stabilising Resistor at the Relay operating current, I_s, is termed the setting voltage, V_s. So that:

$$V_s = I_s \times R_{stab}$$

Note that where high quality CTs are being used, with a high V_k, the value of V_s chosen must not be so low that the CT will be operating at the very low, non-linear part of its magnetising curve.

It is important that R_{stab} is suitably rated to withstand the current levels expected during an internal (in-zone) fault. The continuous rating of R_{stab} should be:

$$\text{Continuous Rating of } R_{stab}\,(W) \geq (I_s)^2 \text{ x } R_{stab}$$

Similarly, R_{stab} must have a short time rating large enough to withstand the fault current levels before the fault is cleared. This is usually for 0.5 seconds to allow for a failure in the main protection system or switchgear and so considers longer fault clearance times through operation of the back-up protection.

$$\text{Short Time Rating of } R_{stab}(W) \geq \frac{V_{MaxSecIntFault}^{\ 2}}{R_{stab}}$$

$$V_{MaxSecIntFault}(V) \geq (V_K^{\ 3} \text{ x } R_{stab} \text{ x } I_{MaxSecIntFault})^{1/4} \text{ x } 1.3$$

Where:

V_k = Kneepoint voltage of the CT

$V_{MaxSecIntFault}$ = Maximum secondary internal fault voltage

$I_{MaxSecIntFault}$ = Maximum secondary internal fault current = $I_{MaxPriIntFault}$ x CT Ratio

Once again, if $I_{MaxPriIntFault}$ is not known, the breaking capacity current of the Circuit Breaker can be used.

Note that the stabilising resistor will have no effect until CT saturation occurs. The CT secondaries act as current sources and any imbalance must go through the relay circuit despite the presence of R_{stab}.

3.2 Non-Linear Resistor

For safety reasons, overvoltages within a protection panel must not be allowed to go above 3kV. For the protection system:

$$V_{Peak}(V) = 2 \text{ x } \sqrt{2 \text{ x } V_K \text{ x } ((I_{MaxSecIntFault} \text{ x } R_{stab}) - V_K)}$$

If V_{peak} can go above 3kV, a Metrosil (non-linear resistor) must be fitted in parallel with the Relay circuit to limit its maximum level. However, it is considered good practice to fit a Metrosil for all installations.

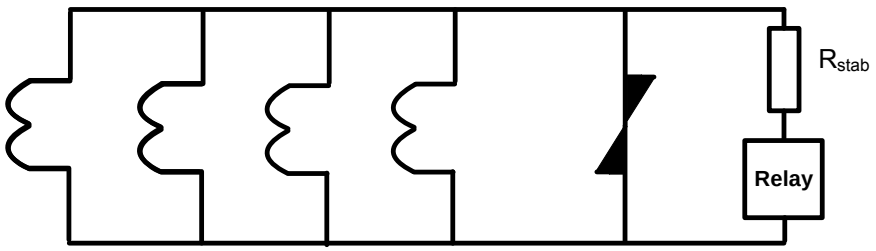


Figure 6 – Non-Linear Resistor

Metrosils are specified by 3 figures – their diameter and the fixed, device-specific constants C (thickness) and β (chemical composition). The diameter relates to the Power Rating of the device, C and B to the current which will flow through the Metrosil for a given voltage:

$$V = C \text{ x } I^{\beta}$$

The voltage characteristic of the Metrosil must be;

Large enough so that negligible current flows through the Metosil at the relay operating voltage.

$$C \text{ x } I_s^{\beta} \gg R_{stab} \text{ x } I_s$$

Small enough so that dangerous over-voltages do not occur.

$$C \times I_{MaxSecIntFault}^{\beta} < 3kV$$

The Metrosil must be rated sufficiently to dissipate the heat created by the flow of maximum secondary internal fault current:

$$\text{Required Continuous Rating of Metrosil (W)} \geq (4 / \pi) \times I_{MaxSecIntFault} \times V_K$$

This will usually give a massive power rating requiring a Metrosil of unrealistic size. For this reason the Metrosil is chosen so that it can withstand $I_{MaxSecIntFault}$ for only the maximum fault clearance time. Generally using the Metrosil's one second rating is sufficient.

3.3 Fault Setting

To achieve correct sensitivity to in-zone faults, the protection scheme must typically operate for a primary current of 10-30% of the minimum primary fault current, $I_{MaxPriIntFault}$.

$I_{MinPriIntFault}$ is a complex figure which must be calculated from a detailed system study.

In addition, allowance must be made for the magnetising current of the paralleled CTs. In effect, these act as losses in the secondary circuit and so reduce the secondary current available to operate the protection.

$$\text{Primary Operate Current} = [(\text{Number of CTs} \times \text{Magnetising Current at } I_s) + I_s] \times \text{CT Ratio}$$

This assumes there is little or no current leakage through the Metrosil or any other current paths.

If this is greater than the maximum allowable Primary operate current of $I_{MinPriIntFault}$ x 30%, then I_s must be reduced to bring it back within specification. This, of course, would entail re-calculating the value of R_{stab}. The process is thus iterative until a suitable primary operate level is achieved.

As the number of paralleled CTs increases, the losses through magnetising current become so large that it becomes impossible to set I_s low enough. At this point the scheme becomes unworkable. As a very rough guideline, the maximum number of paralleled CTs is about 20.

Similarly, if the Primary Operate Current is smaller than the minimum allowable Primary operate current of $I_{MaxPriIntFault}$ x 10%, then I_s must be increased to bring it back within specification.

If it is not possible to increase I_s then a Shunt Resistor, $R_{shunt,}$ can be placed in parallel with the relay. This has the effect of modifying the above equation to:

$$\text{Primary Operate Current} = [(\text{Number of CTs} \times \text{Magnetising Current at } I_s) + I_s + I_{shunt}] \times \text{CT Ratio}$$

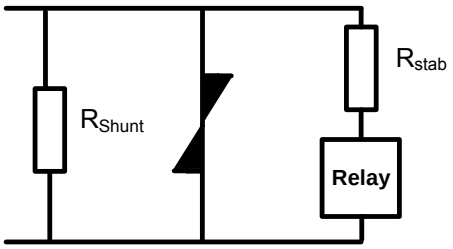


Figure 7 – Shunt Resistor

The value of R_{shunt} can then be calculated:

$$I_{shunt} \geq (\text{Primary Operate Current} / \text{CT Ratio}) - [(\text{Number of CTs} \times \text{Magnetising Current at } I_s) + I_s]$$

$$R_{shunt} \leq (I_s \times R_{stab}) / I_{shunt}$$

For solidly earthed systems, where the fault current will be very high, it is acceptable practice to use a primary fault setting of 50% of the Busbar full load current.

3.4 Check Zone

On double busbar systems, where there will be a significant number of switching operations, it is usual to provide an extra level of tripping security by fitting a Check Zone relay. This monitors the current of every incomer and outgoing feeder on the Busbar, but not the internal Busbar Sections and Couplers.

A Check Zone relay is also sometimes installed on single busbar systems of high importance.

The outputs of the relays protecting each Busbar zone are then connected in series with the Check Zone relay's outputs. Only when both operate will a trip be issued.

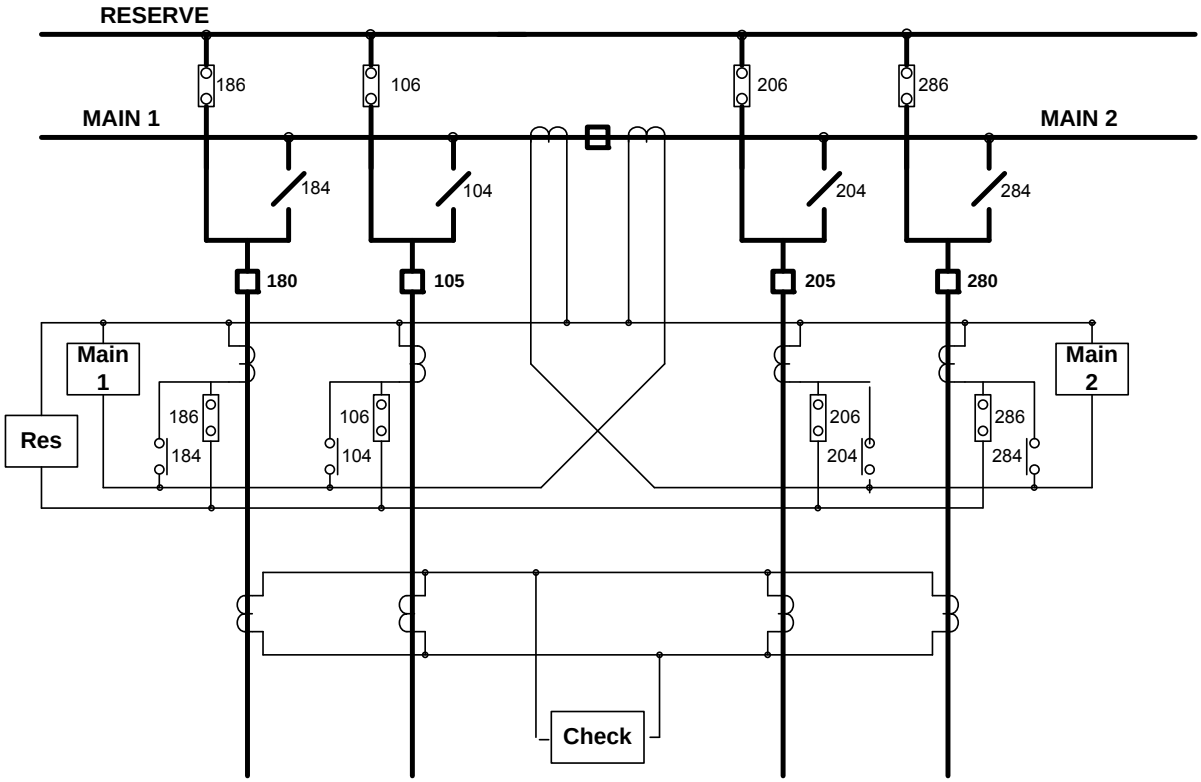


Figure 8 – Check Zone Relay

4. Current Transformer Requirements

The CTs used in a High-Impedance Differential scheme must follow some simple rules:

- They must be of the high-accuracy type in accordance with Class 'PX' to IEC 60044.
- They must have the same turns ratio.
- The knee point voltage of each CT should be at least 2 x Vs.

  The knee point voltage is expressed as the voltage applied to the secondary circuit with the primary open circuit which when increased by 10% causes the magnetising current to increase by 50%.

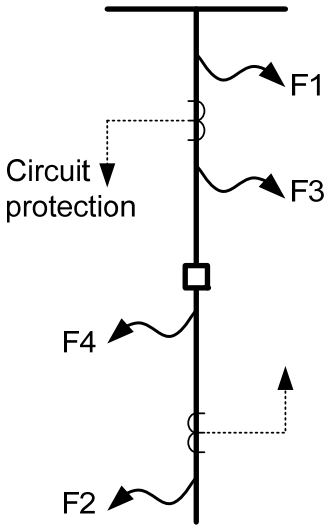
It is permissible for the CTs to have different magnetizing characteristics since under load (or through-fault) conditions the secondary currents will substantially balance. For an in-zone fault, there will be high levels of secondary current and so any unbalance in the magnetizing characteristics will actually aid correct tripping.

5. Current Transformer Location

The mounting position of CTs for busbar protection varies according to the type of switchgear. In many cases, the CTs are built into the Circuit Breakers. In others, they are separate devices located as close to the Breakers as possible.

5.1 CTs overlapping the Circuit Breaker

This arrangement is common in outdoor bulk oil types. The performance of the protection is considered for the faults F1 to F4.



A fault at F1 is a busbar fault which should be cleared by the busbar protection.

Fault F2 is a circuit fault and should be cleared by the circuit protection.

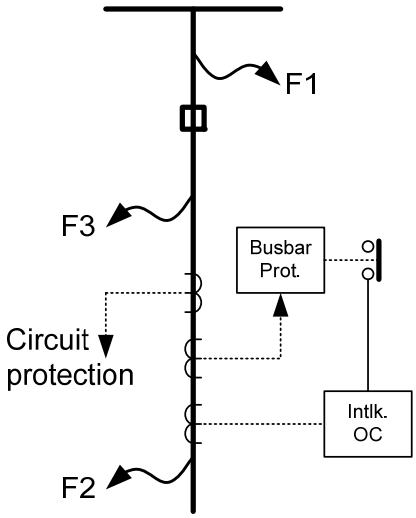
F3 is a busbar fault but because of its position should cause both busbar and circuit protection to operate and the fault will be cleared, although the circuit breaker at the remote end of the circuit may also be tripped.

Although F4 is a circuit fault, it may be detected by both circuit and busbar protection depending on their relative operating times. Thus, circuit breakers selected to the busbar may be opened unnecessarily for a circuit fault.

For F3 and F4, the disadvantage may be acceptable in view of the low incidence of such faults.

Figure 9 – CTs Overlapping the CB

5.2 CTs on the circuit side of the Circuit Breaker



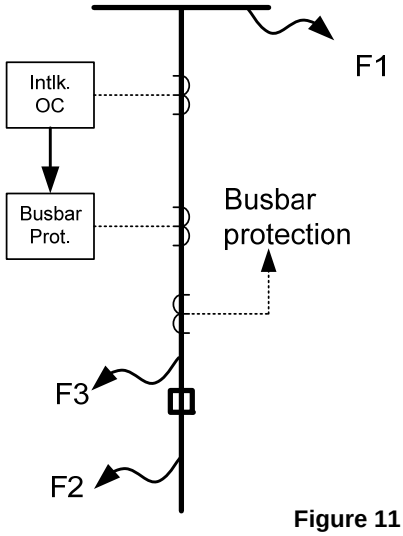
Faults F1 and F2 should be correctly cleared as before, but F3 will only cause operation of the busbar protection because the fault is outside the circuit protection zone. Thus the fault may remain fed from the remote end of the circuit. Arrangements must therefore be made to cause the CB at the remote end of the line to be tripped under these circumstances.

This can be affected by a direct intertrip or CB fail scheme. Another method, as shown, uses an interlocked overcurrent relay. This is arranged to detect any power infeed at F3 after the circuit breaker is opened.

This relay is a three pole over current type with a time setting of about 0.3 second. Its operation is inhibited until the busbar protection operates and so if the fault persists at F3 after the circuit breaker opens, the busbar protection remains operated, so permitting the interlocked overcurrent relay to function and unstabilise the circuit unit protection or send an intertripping signal to the remote end of the circuit.

Figure 10 – CTs on other side of CB

5.3 CTs on the Busbar side of the Circuit Breaker



The faults at F1 and F2 will be correctly cleared.

A fault at F3 will cause the circuit protection to trip the circuit breaker, but the fault will remain fed from the busbars. The busbar protection will not operate as F3 is outside its zone.

Again an interlocked Over current relay is used, but in this case, since it is the circuit protection which remains operated for the fault at F3, it is this protection which is used to initiate operation of the interlocked overcurrent relay. If F3 persists for about 0.3 seconds, the interlocked overcurrent relay then operates the tripping relays of the protection of the section of busbar to which the circuit is selected.

Figure 11 – CTs on Busbar side of CB

5.4 Bus Section and Bus Couplers

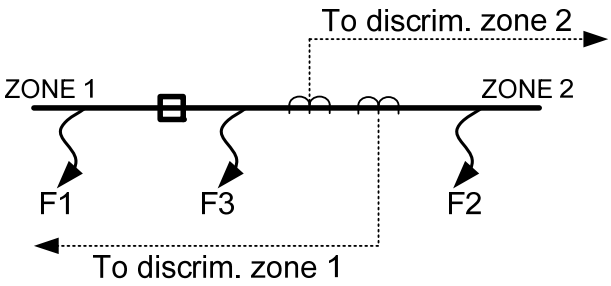


Figure 12 – CTs on Bus Section and Bus Coupler

For these, the ideal arrangement is to have a set of CTs on each side of the circuit breaker. The CTs associated with a discriminating zone should be mounted on the side of the breaker away from the zone with which they are associated.

If the two sets of CTs are mounted on one side as shown, then faults F1 and F2 will be correctly cleared by the operation of the appropriate discrimination zone relays plus the overall check relay. A fault at F3 will cause the operation of zone discrimination relay plus the check relay to clear the left hand busbar. However, F3 will continue to be fed from the circuits selected to zone 2 busbar, since the zone 2 busbar protection will not operate as this fault is just outside its zone. For such a fault at F3, the zone 1 relay will clear the busbar and reset, so de-energising relay TD before it has time to operate the zone 2 trip relay. Relay TD must therefore have a setting time of about 0.4 seconds. Similar considerations apply in the case of Bus Couplers.

6. CT Supervision

If a CT secondary becomes open-circuit, or if the wiring to the CT is broken, a current unbalance will be created in the Relay circuit. This may exceed the operating level in which case the protection has no option but to cause a trip.

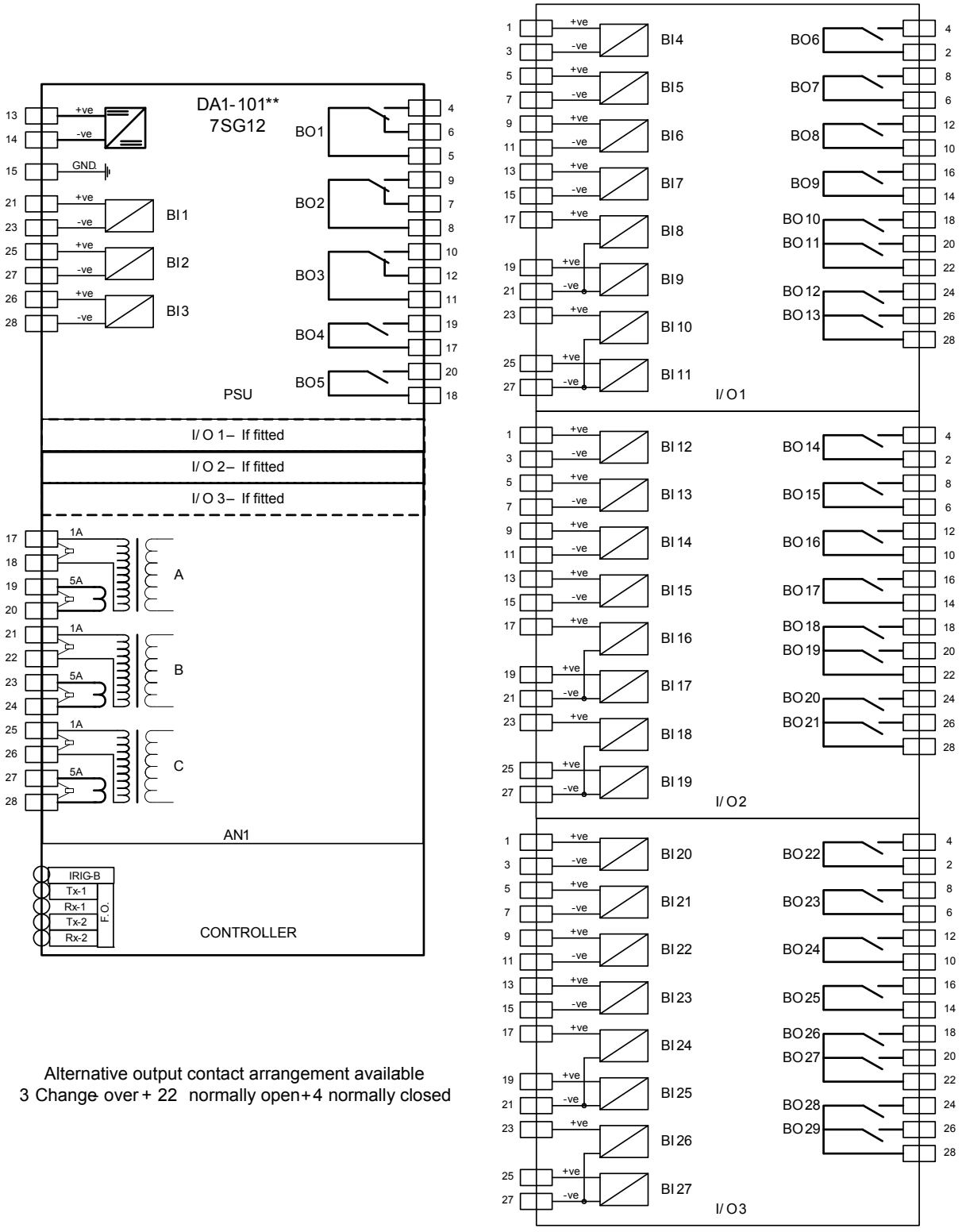
If the resulting unbalance is lower than the operate level, however, it is important that the condition is detected since a resulting through fault may be sufficient to raise the unbalanced current above the operate level. A simple current pick-up is therefore provided, CT Supervision, which should be set higher than normal unbalance levels due to measuring errors, etc. but lower than the Differential operate level. Generally a setting of 10% of the Differential operate level is acceptable.

Once a CT Supervision condition has been detected, the relay can be programmed to issue an alarm via one of the output contacts. Where a mal-operation is preferred to missing a real fault, this alarm is used to simply alert the system operator to the condition. It should then be rectified as soon as possible.

Where a mal-operation is unacceptable, however, this alarm can be used to disable the protection until the CT is repaired. Traditionally this has been done by using the alarm to short-circuit the secondaries of all the CTs for a given phase, since there is no way of telling which is faulty. This method has been used where an open-circuited CT may cause damage to plant. Care must be taken, however, to ensure that the rating of the relay output contacts is sufficient to make and break the high current transients involved. If not, the alarm output must be used to operate a dedicated shorting relay with higher-rated contacts.

With modern numeric relays like the DAD-N, it has become possible to simply disable the Differential protection rather than short out the CT secondaries. To do this, the CT Supervision alarm output contact should be externally connected to a status input used to inhibit the relay's Differential protection elements.

Note that the CT Supervision delay must be set carefully. Since the CT Supervision element will still pick-up for a genuine fault condition, the delay should be set long enough so that it does not issue an alarm before the protection has correctly cleared the fault. Setting the delay too low (less than a few seconds) may cause confusion where the CT Supervision condition is used as an alarm, and an unacceptable race condition where the CT Supervision alarm is used to disable the protection (will the protection operate to clear the genuine fault before the CT Supervision alarm disables it ?) Typically a setting of 2 to 10 seconds is applied.



Alternative output contact arrangement available
3 Change- over + 22 normally open+4 normally closed

Figure 13 – DAD-N Connection Diagram

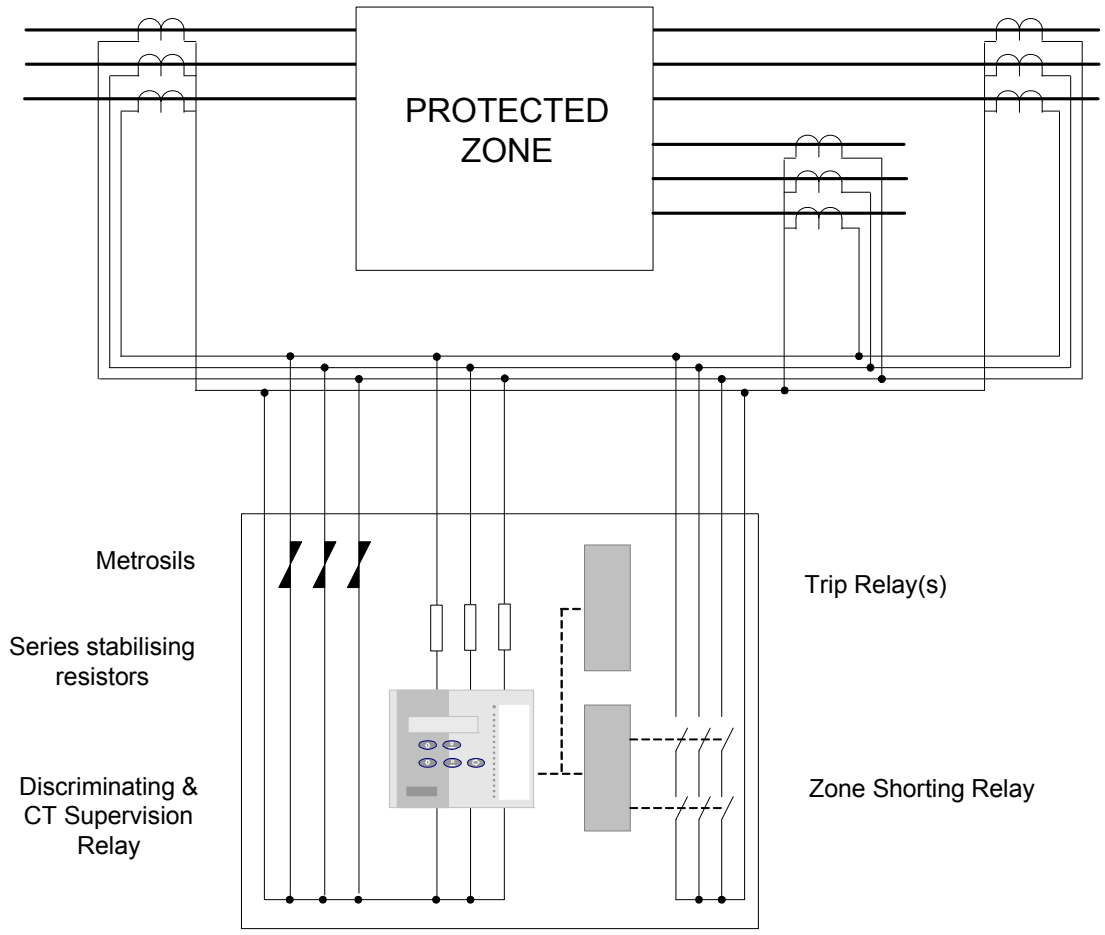


Figure 14 – Typical High Impedance Protection Components

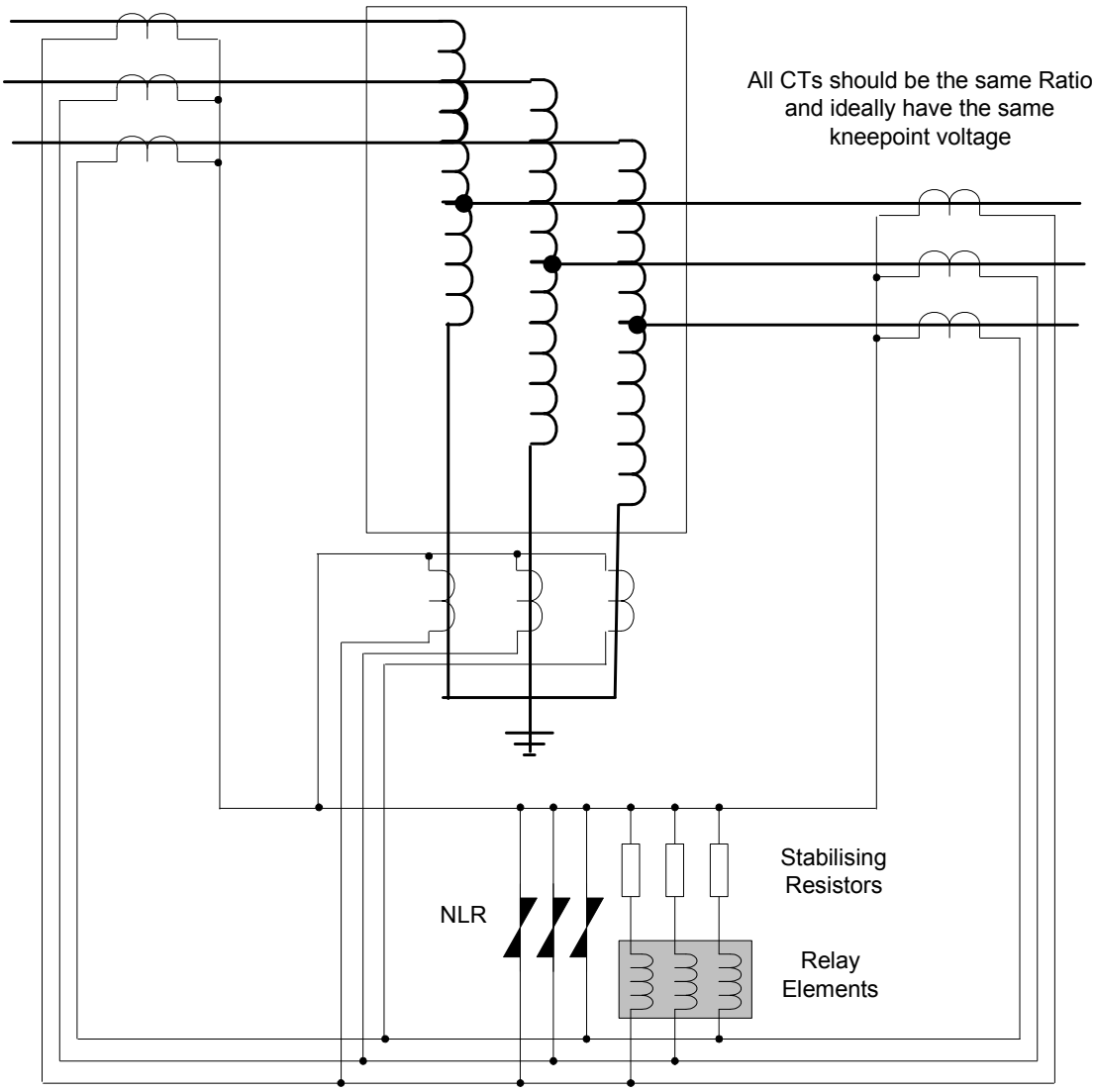


Figure 15 – High Impedance Protection of Auto-transformer

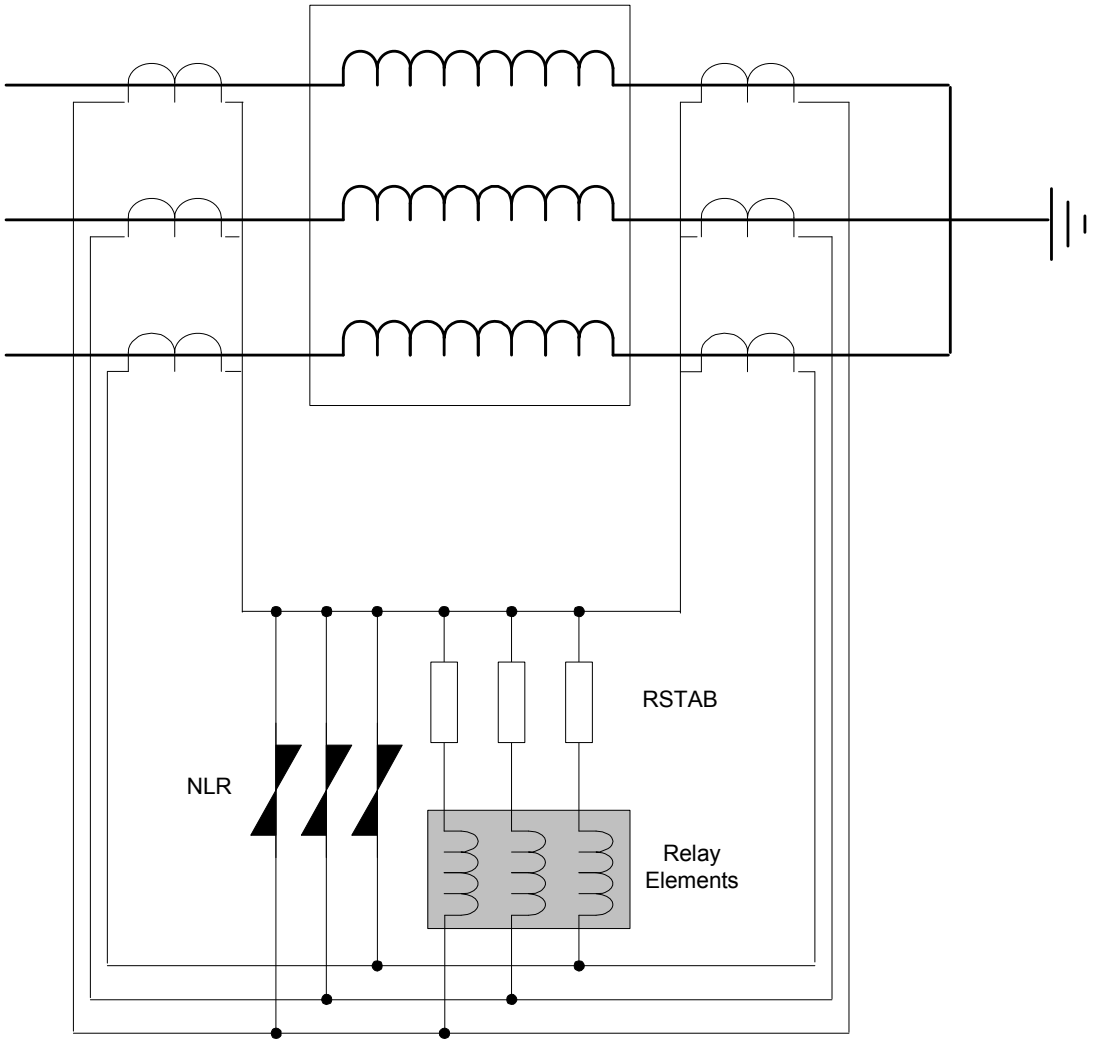


Figure 16 – High Impedance Protection of Motor, Generator or Reactors

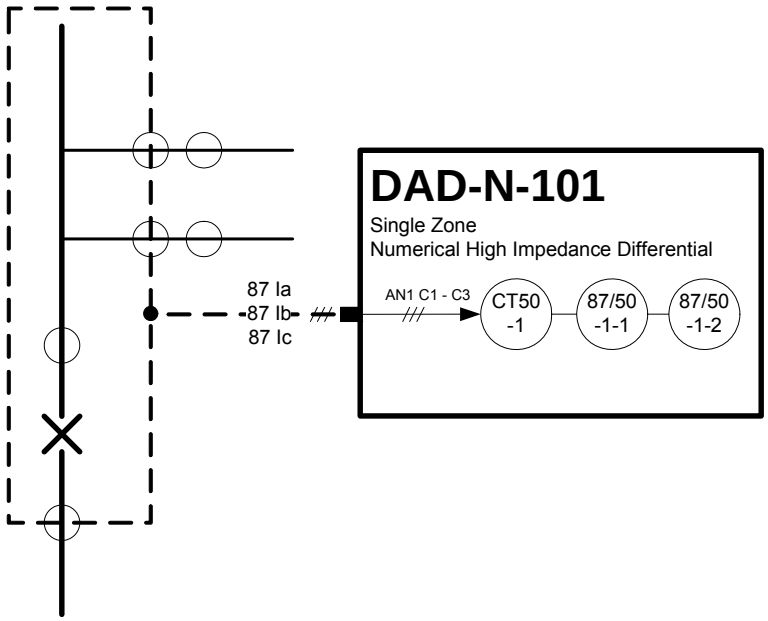


Figure 17 – DAD-N-101 Differential Protection Elements